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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,920	05/03/2005	Peter Nicholls	P/63610	5427
156 7590 12/31/2007 KIRSCHSTEIN, OTTINGER, ISRAEL & SCHIFFMILLER, P.C. 489 FIFTH AVENUE NEW YORK, NY 10017			EXAMINER SEDIGHIAN, REZA	
			ART UNIT 2613	PAPER NUMBER
			MAIL DATE 12/31/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/506,920	Applicant(s) NICHOLLS ET AL.	
	Examiner M. R. Sedighian	Art Unit 2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 18-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 18, 19 and 25-33 is/are rejected.
- 7) ☒ Claim(s) 20-24 and 34 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>9/3/04</u> . | 6) <input type="checkbox"/> Other: _____ |

1. This communication is responsive to applicant's preliminary amendments of 9/3/04. The amendments have been entered. Claims 18-34 are now pending.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-19 and 25-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Traa (US Patent No: 6,222,660 B1).

Regarding claims 18 and 25, Traa teaches a method of controlling a bias voltage of an avalanche photodiode (col. 1, lines 1-10) in an optical communications system (col. 2, lines 55-60 and fig. 1) including forward error correction (col. 2, lines 55-63), the method comprising the steps of: a) measuring an error rate (32, fig. 1) in an electrical signal converted from an optical signal by the avalanche photodiode (APD, fig. 1) over a plurality of sample periods (col. 2, lines 59-64, col. 4, lines 3-7); and adjusting (18, fig. 1) the bias voltage (V_{APD} , fig. 1 and col. 2, lines 40-54, 56-67) applied to the avalanche photodiode (APD, fig. 1) to minimize the error rate in the electrical signal by determining whether the error rate is increasing or decreasing with time (col. 3, lines 1-21 and fig. 2). As to claim 25, Traa discloses an error rate measurer (32, fig. 1), an adjustment circuit (18, fig. 1), and a decision logic (the decision logic of the bit error rate counter 32).

Regarding claims 19 and 26, Traa discloses determining the bias voltage by a value of a counter which is incremented or decremented every sample period and changing a count

direction of the counter if the error rate is increasing with time (col. 3, lines 8-20, note that it is well known that a BER counter, such as BER counter 32 can increment or decremented a count value in different sample periods and can change the count direction of the counter if the error rate is increasing with time).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traa (US Patent No: 6,222,660 B1) in view of Reed, Jr. (US Patent No: 6,421,077 B1).

Regarding claim 27, Traa differs from the claimed invention in that Traa does not specifically disclose the means for changing the count direction is a toggle. However, it is well known that a BER counter such as the one of Traa counts the number of toggles. For example, Reed discloses a counter (130, 136, fig. 1) that counts the number of toggles (errors, col. 4, lines 20-30). As it is taught by Reed and as it is well known, it would have been obvious to a person of ordinary skill in the art at the time of invention that an error rate counter such the one of Traa can toggle to effectively detect the bit error rate from the transmitted digital data signal.

Regarding claim 28, Traa further discloses a digital to analog converter (DAC, fig. 1) for converting the counter value (col. 2, lines 30-35) to an analog APD bias voltage (V_{APD} , fig. 1).

6. Claim 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Traa (US Patent No: 6,222,660 B1) in view of Reed, Jr. (US Patent No: 6,421,077 B1) and in further view of Tanaka Masataka (Japanese Patent No: 2-230834).

Regarding claim 29, the modified error rate detection system of Traa and Reed differ from the claimed invention in that Traa and Reed do not disclose the adjustment circuit comprises an error pulse counter for counting error pulses over a predetermined interval and a store for holding error counts for a plurality of earlier intervals. Tanaka Masataka discloses an error pulse counter (11, fig. 1) for counting error pulses over a predetermined interval (see abstract) and a store (13, fig. 1) for holding error counts for a plurality of intervals (see abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate an error pulse counter and storing circuitries such as the ones of Tanaka Masataka for the BER counter of Traa to detect and store different error signals of the transmitted data over predetermined time periods.

Regarding claim 30, Tanaka Masataka further discloses a decision logic (BER 12, fig. 1) that operates on the error counts held in the store (see abstract).

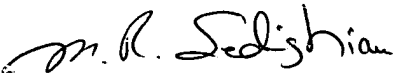
Regarding claims 31-33, as to varying the interval over which error pulses are counted, or varying the interval in dependence on the error rate, or varying the interval between a plurality of different interval lengths, it is well known that bit error rate counters, such as the ones of Traa or Tanaka Masataka each can detect and count the error signals at different timing intervals or at varying intervals to further calculate an efficient and accurate BER output signal that can be further used for signal processing, measurement, and/or control.

7. Claims 20-24 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. R. Sedighian whose telephone number is (571) 272-3034. The examiner can normally be reached on 9 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


M. R. SEDIGHIAN
PRIMARY EXAMINER